AMENDMENTS TO THE CLAIMS

1. (Original) A multi-chip package comprising:

a first semiconductor chip coupled with a first electrode plate; and

a second semiconductor chip coupled with a second electrode plate, the first electrode plate and the second electrode plate arranged to provide a decoupling capacitor between the first semiconductor chip and the second semiconductor chip.

2. (Original) The multi-chip package of claim 1, further comprising first rerouting lines coupled with the first semiconductor chip, wherein the first semiconductor chip, first electrode plate, and the first rerouting lines constitute part of a first rerouted chip.

3. (Original) The multi-chip package of claim 1 wherein the package is a Ball Grid Array (BGA) package.

4. (Original) The multi-chip package of claim 2, wherein the first semiconductor chip further comprises first chip pads.

5. (Original) The multi-chip package of claim 4, wherein the first chip pads include first power chip pads.

6. (Original) The multi-chip package of claim 4 wherein the first chip pads include first ground chip pads.

7. (Original) The multi-chip package of claim 4, wherein the first rerouting lines are on the first semiconductor chip and electrically connect with the first chip pads.

8. (Original) The multi-chip package of claim 7, wherein the first electrode plate is on the first semiconductor chip and electrically connects with the first chip pads.

9. (Original) The multi-chip package of claim 8, further comprising second rerouting lines coupled with the second semiconductor chip, wherein the second semiconductor chip, second electrode plate, and second rerouting lines constitute part of a second rerouted chip.

10. (Original) The multi-chip package of claim 9, wherein the second semiconductor chip further comprises second chip pads electrically connecting with first chip pads.

11. (Original) The multi-chip package of claim 10, wherein the first electrode plate connects with first power chip pads and the second electrode plate connects with second ground chip pads.

12. (Original) The multi-chip package of claim 10, wherein the first electrode plate connects with first ground chip pads and the second electrode plate connects with second power chip pads.

13. (Original) The multi-chip package of claim 10, further comprising a plurality of first interconnection bumps to electrically connect the first rerouting lines and the second rerouting lines.

14. (Original) The multi-chip package of claim 13, further comprising a substrate to fixedly support the first rerouted chip.

15. (Original) The multi-chip package of claim 14, further comprising a plurality of bonding wires to electrically connect the first rerouting lines with the substrate.

16. (Original) The multi-chip package of claim 15, further comprising a plurality of conductive balls arranged under the substrate to electrically connect the substrate to electronics.

17. (Original) The multi-chip package of claim 16, wherein the first rerouted chip further includes a first insulating layer on the first semiconductor chip, the first insulating layer comprising the first electrode plate.

18. (Original) The multi-chip package of claim 17, wherein the first insulating layer has first openings, the first electrode plate to communicate with the first chip pads through the first openings.

19. (Original) The multi-chip package of claim 18, wherein the first electrode plate is coplanar with the first rerouting lines.

20. (Original) The multi-chip package of claim 19, wherein the first electrode plate has first slots.

21. (Original) The multi-chip package of claim 20, wherein the first rerouting lines are within the first slots.

22. (Original) The multi-chip package of claim 21, wherein the first rerouting lines have a coplanar waveguide to control impedance.

23. (Original) The multi-chip package of claim 22 wherein the impedance is controlled according to a ratio of a width of the first rerouting line to a width of the first slot.

24. (Original) The multi-chip package of claim 16, wherein the second rerouted chip further includes a second insulating layer on the second semiconductor chip, the second insulating layer comprising the second electrode plate.

25. (Original) The multi-chip package of claim 24, wherein the second insulating layer has second openings, the second electrode plate to communicate with the second chip pads through the second openings.

26. (Original) The multi-chip package of claim 16, wherein the second electrode plate is coplanar with the second rerouting lines.

27. (Original) The multi-chip package of claim 26, wherein the second electrode plate has second slots.

28. (Original) The multi-chip package of claim 27, wherein the second rerouting lines are disposed within the second slots.

29. (Original) The multi-chip package of claim 28, wherein the second rerouting lines have a coplanar waveguide to control impedance.

30. (Original) The multi-chip package of claim 29 wherein the impedance is controlled according to a ratio of a width of the second rerouting line to a width of the second slot.

31. (Original) The multi-chip package of claim 16, wherein the first rerouted chip further includes a third electrode plate opposite the second electrode plate with respect to the first electrode plate, to electrically connect with the first chip pads.

32. (Original) The multi-chip package of claim 16, wherein the second rerouted chip further includes a fourth electrode plate opposite the first electrode plate with respect to the second electrode plate, to electrically connect with the second chip pads.

33. (Original) The multi-chip package of claim 16, further comprising:

a plurality of second interconnection bumps to electrically connect the first rerouting lines and the second rerouting lines, the plurality of second interconnection bumps adjacent to and spaced from the first interconnection bumps.

34. (Original) A multi-chip package comprising:

a first rerouted chip including a first semiconductor chip with first chip pads, and first rerouting lines on the first semiconductor chip to electrically connect with the first chip pads, each first rerouting line having a first bump pad, a third bump pad, and a bond pad;

a second rerouted chip facing the first rerouted chip including a second semiconductor chip having second chip pads, and second rerouting lines disposed on the second semiconductor chip to electrically connect with the second chip pads, each second rerouting line having a second bump pad and a fourth bump pad;

a plurality of first interconnection bumps between and electrically connecting the first bump pad and the second bump pad;

a plurality of second interconnection bumps between and electrically connecting the third bump pad and the fourth bump pad;

a substrate fixedly supporting the first rerouted chip;

a plurality of bonding wires disposed on the respective bond pads to electrically connect the first rerouting lines with the substrate; and

a plurality of conductive balls under the substrate to electrically connect the substrate to electronics.

35. (Original) The multi-chip BGA package of claim 34, further comprising:

a plurality of dummy balls between the first rerouted chip and the second rerouted chip.

36. (Withdrawn) A method comprising:

forming a first insulating layer on a first semiconductor chip, exposing first chip pads;

sputtering a first under bump metal layer on the first insulating layer;

plating a first electrode plate and first rerouting lines on the first under bump metal layer, the first electrode plate separated from the first rerouting lines;

partially removing the first under bump metal layer;

connecting the first rerouting lines with the corresponding first chip pads through the first under bump metal layer; and

connecting the first electrode plate to first ground chip pads among the first chip pads, to make a first rerouted chip.